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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,898	02/20/2002	Osamu Hirabayashi	005405.00005	3064

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EXAMINER	
BONZO, BRYCE P	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,898	HIRABAYASHI, OSAMU	
	Examiner	Art Unit	
	Bryce P Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/20/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-6 and 10 are rejected under 35 USC §102.

Claims 7-9 and 11 are rejected under 35 USC §103.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Cirimele (United States Patent No. 4,245,212).

As per claim 1, Cirimele discloses:

A semiconductor memory configured such that it can be connected with a first and second timing generator, the semiconductor memory comprising:

a first register configured to communicate with a memory array and the first timing generator, to retrieve and to hold first data from the memory array at a first timing (column 2, lines 32-34 describe the register and memory array; column 2, lines 16-31 describe the timing generator) ;

a logic gate configured to communicate with the memory array and the first register, to receive the first data from the first register and second data from the memory array after the first timing, so as to compare the first and second data with each other, so that it can provide a comparison result indicating whether or not the first and second data agree with each other (column 1, lines 38-37); and

a second register configured to communicate with the logic gate and the second timing generator, to retrieve and to hold the comparison result at a second timing (column 2, lines 16-31; column 3, lines 10-22).

As per claim 2, Cirimele discloses:

further comprising a flip-flop circuit configured to communicate with the second register, and to hold a data disagreeing state if even one of the comparison results in the second register indicates that the first and second data disagree with each other (column 2, lines 48-52).

As per claim 5, Cirimele discloses:

the first timing is provided when output data is definite (the system of Cirimele only deals with definite data, and never discloses the handling of ambiguous data); and

the second timing is changed at intervals of clock cycles (the system of Cirimele discloses the operation based on clock edges Figure 3).

As per claim 6, Cirimele discloses:

the second timing is provided when output data is definite(the system of Cirimele only deals with definite data, and never discloses the handling of ambiguous data); and

the first timing is changed at intervals of clock cycles (the system of Cirimele discloses the operation based on clock edges Figure 3).

As per claim 3, Cirimele discloses:

a first register configured to communicate with a memory array and the first timing generator, to retrieve and to hold first data from the memory array at a first timing (Figure 1, item 12);

a second register configured to communicate with the memory array and the second timing generator, to retrieve and to hold second data from the memory array at a second timing (Figure 1, item 20);

a delay circuit configured to communicate with the second timing generator, so as to delay the second timing, so that it can provide a third timing (Figure 1, item 22);

a logic gate configured to communicate with the first and second register, to receive the first data from the first register and the second data from the second register, so as to compare the received first and second data with each other, so that it can provide a comparison result indicating whether or not the first and second data agree with each other (column 2, lines 1-15); and

a third register configured to communicate with the delay circuit and the logic gate, to retrieve and to hold the comparison result at the third timing (column 1, item 28).

As per claim 10, Cirimele discloses:

wherein the first register receives a clock signal instead of the first data (figure 2B shows a clock signal on line QC being supplied to the data memory 12)

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cirimele (United States Patent No. 4,245,212).

As per claims 7-9, Cirimele does not explicitly disclose:

the first timing is provided in response to rising or falling edge of a first strobe signal; and

the second timing is provided in response to falling or rising edge of a second strobe signal.

Official Notice is given that it is notoriously well to implement the output of a timer as a strobe. Strobes are signals which indicate a status change. They are very fast line state changes that convey a simple concept. They are often used for clocking, as they

convey the simple concept of advancing time. Thus it would have been obvious to one of ordinary skill in the art of circuit design to implement the clocking and timing mechanisms of Cirimele into strobes as a known in the prior art, thereby creating a high speed timing mechanism to keep up modern computing.

As per claim 11, Cirimele does not discloses:

an output of the flip-flop circuit is supplied to a shift register of a boundary scan circuit. Official Notice is given that is well known to provide any data in a processor to a boundary scan circuit. Boundary scans are a well known method to view the internal states of processor and are used in a variety of diagnostics. Thus it would have been obvious to one of ordinary skill at the time of invention to provide access to the flip flop circuit of Cirimele to a boundary scan circuit, thus allowing the circuitry to be diagnosed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703) 305-4834 or upon moving to the new facilities in Alexandria (571) 272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713 or upon moving to the new facilities in Alexandria (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Examiner
Art Unit 2114

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